**REPORT ON ECE PROJECT**



**BTech/ II Year CSE/ III Semester**

**19ECE282/ Digital Electronics and Systems Lab**

**Final Project Review (Report)**

|  |  |
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**2022 -2023 Odd Semester**

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**Question:**

An automobile speed sensor provides a 4-bit encoded reading S3 S2 S1 S0 in intervals of one. Design a decoder with the following outputs

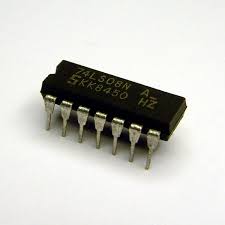
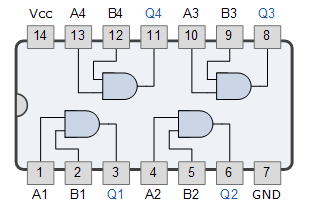
1. Slow, denoted by s which is asserted when the sensor output is between 0 and 5.
2. Economy, denoted by e which is asserted when the sensor output is between 6 and 12
3. Fast, denoted by e which is asserted when the sensor output is between 13 and 15
4. Design a decoder for the above system.
5. Design a circuit for displaying “S”, “E” and “F” in a 7 segment display when the respective outputs s, e and f are asserted.

**Components Used:**

* Quad AND Gate (IC7408) – 2
* Quad OR Gate (IC7432) – 2
* Quad XOR Gate(IC7486) – 1
* NOT Gate(IC7404) - 2
* Triple 3-input AND Gate (IC7411) – 1
* 7 Segment Display – 1
* Resistor (1 k-ohm) – 2
* Breadboard – 1
* Digital IC Trainer – 1
* Connecting wires – as required

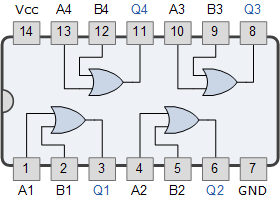
**Details of Hardware Used:**

1. Quad AND Gate (IC7408) –

IC7408 contains four independent gates each of which performs the logic of 2-input AND gate. It comes in 14-pin DIP package. The AND gate consists of two inputs and only one output. The ouput returns high when both the inputs are high, otherwise it will return low.

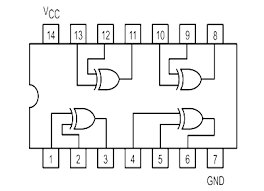
1. Quad OR Gate (IC7432) –

IC7432 has the functionality of OR gate. It has four OR gates of two inputs and one output in one package. It will give high if either all or any of the input is high.It produce low only when both of the inputs are low.



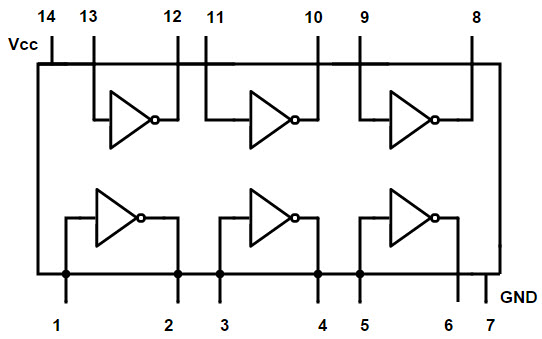
1. Quad XOR Gate(IC7486) –

“XOR” an abbreviation for “Exclusively-OR.” The simplest XOR gate is a two-input digital circuit that outputs a logical “1” if the two input values differ, i.e., its output is a logical “1” if either of its inputs are 1, but not at the same time (exclusively).

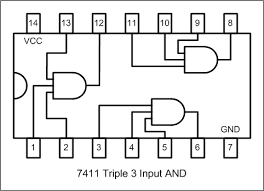
 

1. NOT Gate(IC7404) –

The NOT gate is an electronic circuit that produces an inverted version of the input at its output.  It is also known as an *inverter*.  If the input variable is A, the inverted output is known as NOT A.

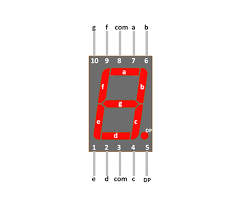
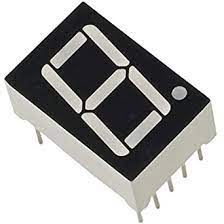
 

1. Triple 3-input AND Gate (IC7411) –

74LS11 triple 3-input AND gate IC is a 14-pin DIP package. The 74LS11 contains three independent gates each of which performs the logic AND function, i.e., it returns high only when all the inputs are high and for all cases it will return low.

1. 7 Segment Display –

The 7-segment display consists of seven LEDs arranged in a rectangular fashion. Each of the seven LEDs when illuminated the segment forms part of a numerical digit to be displayed. An additional 8th LED is sometimes used within the same package allowing the indication of a decimal point, (DP) when two or more 7-segment displays are connected together to display numbers greater than ten.



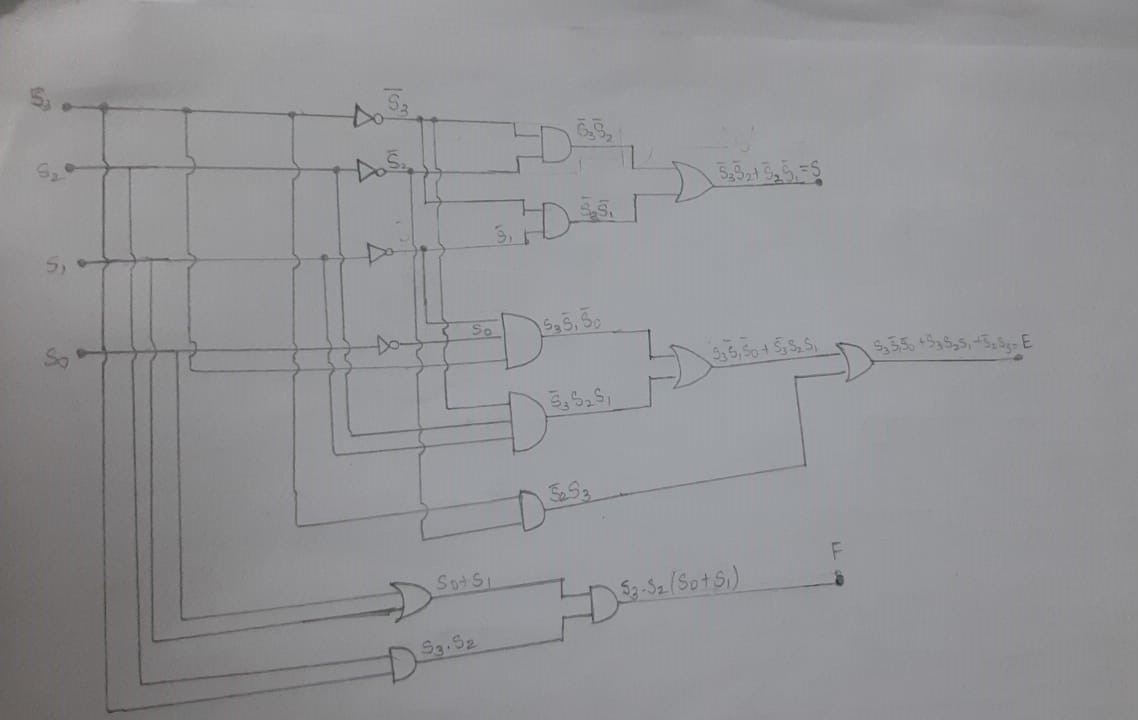
1. Resistor (1 k-ohm) –

A resistor is an electrical component that limits or regulates the flow of electrical current in an electronic circuit. Resistors can also be used to provide a specific voltage for an active device such as a transistor.

**Design Diagram:**

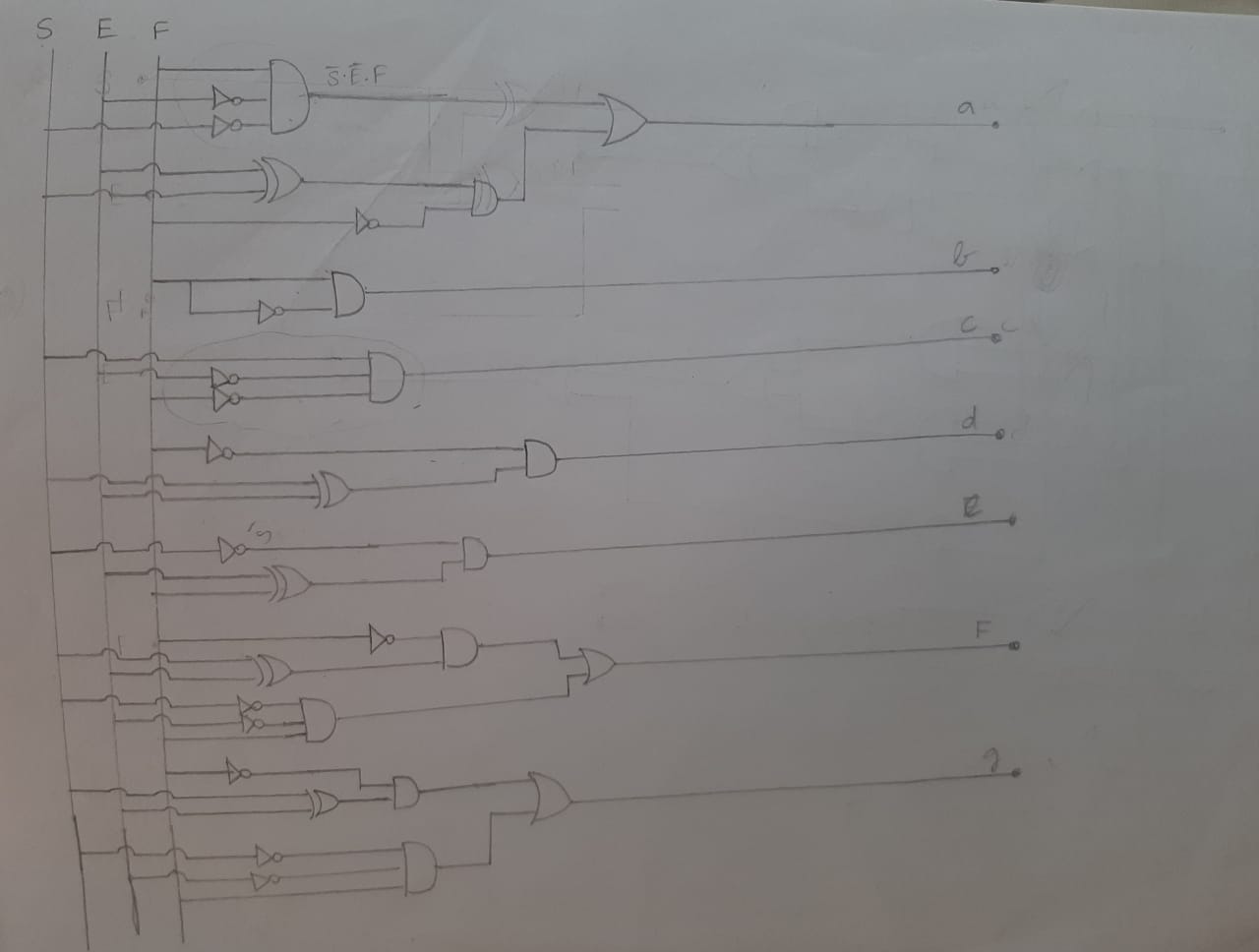
1. For Triggering S,E,F :-

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| S3 | S2 | S1 | S0 |  | S | E | F |
| 0 | 0 | 0 | 0 |  | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 |  | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |  | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |  | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 |  | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |  | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |  | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 |  | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 |  | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 |  | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |  | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 |  | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |  | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |  | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |  | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 |  | 0 | 0 | 1 |



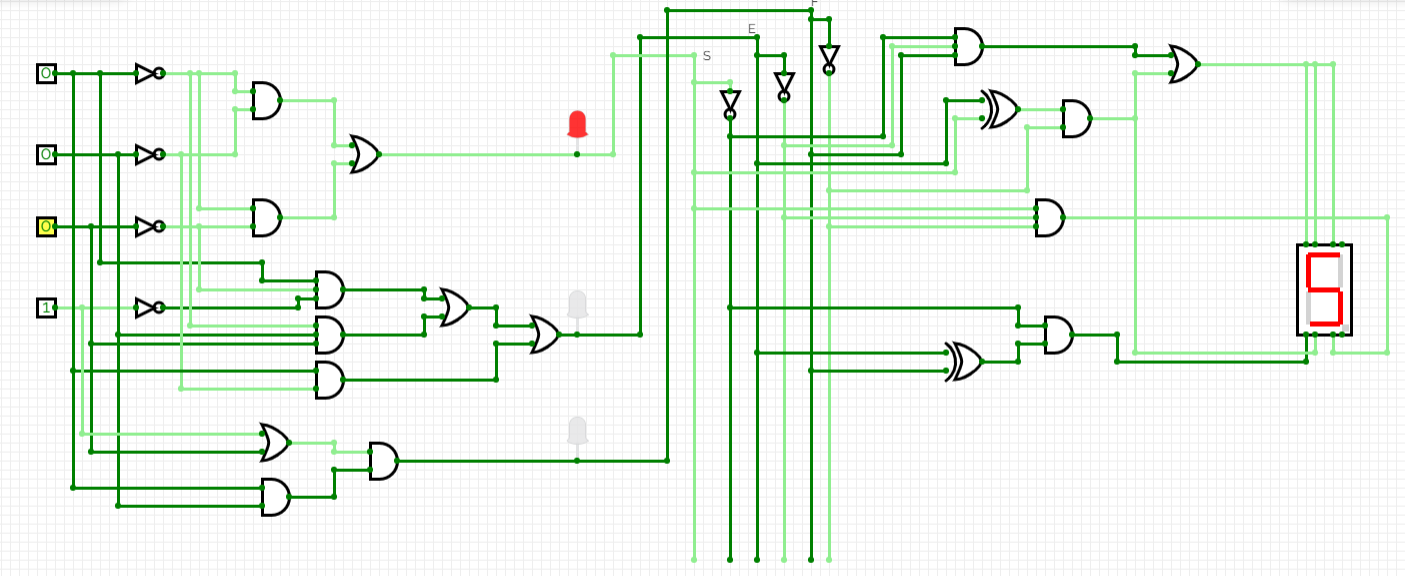
1. For 7 Segment Display :-

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| S | E | F |  | a | b | c | d | e | f | g |
| 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 |  | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 |  | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 |  | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

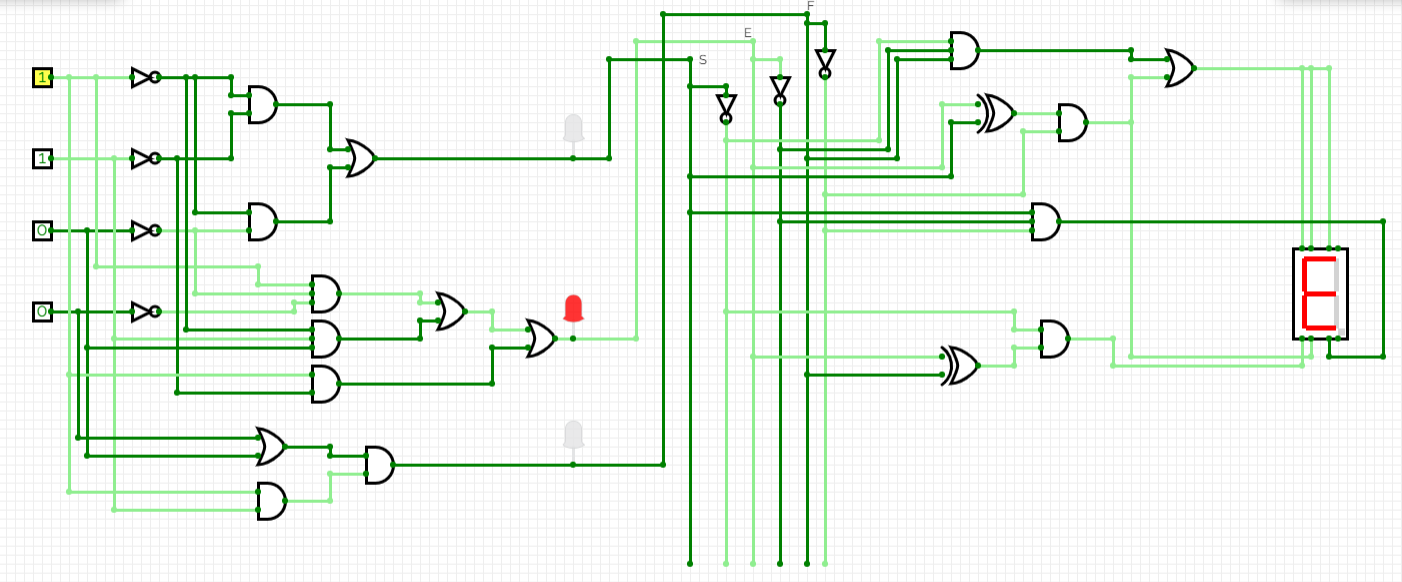


**Simulation Results:**

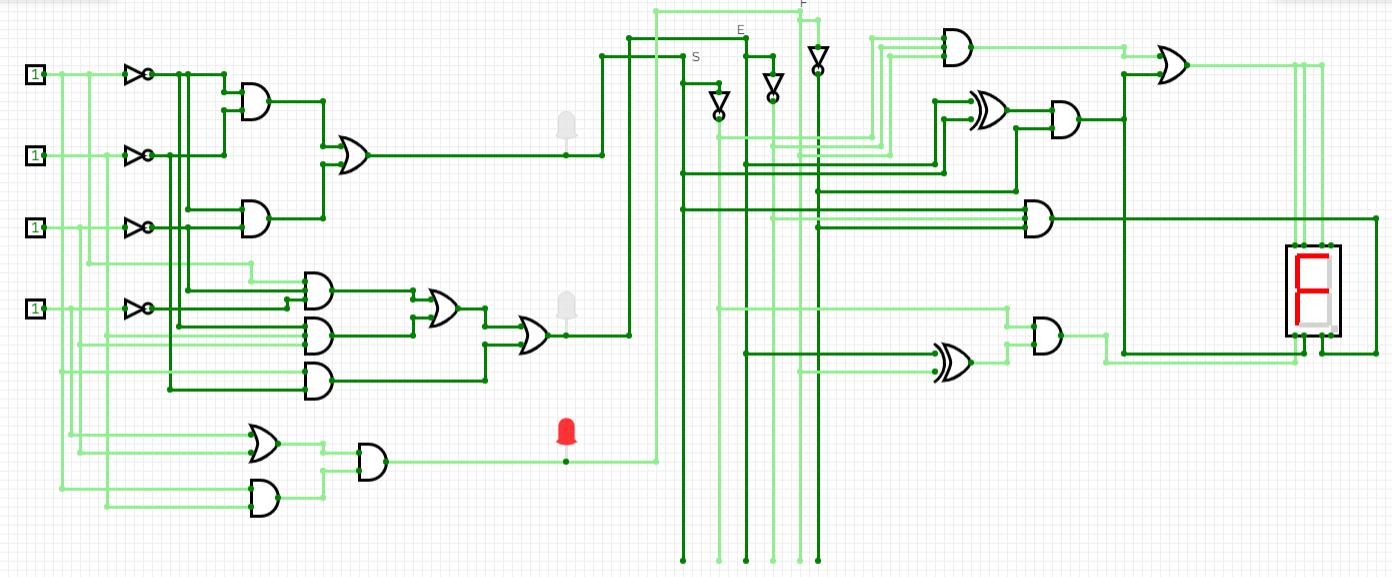
1. *Case 1 –*



1. *Case 2 –*

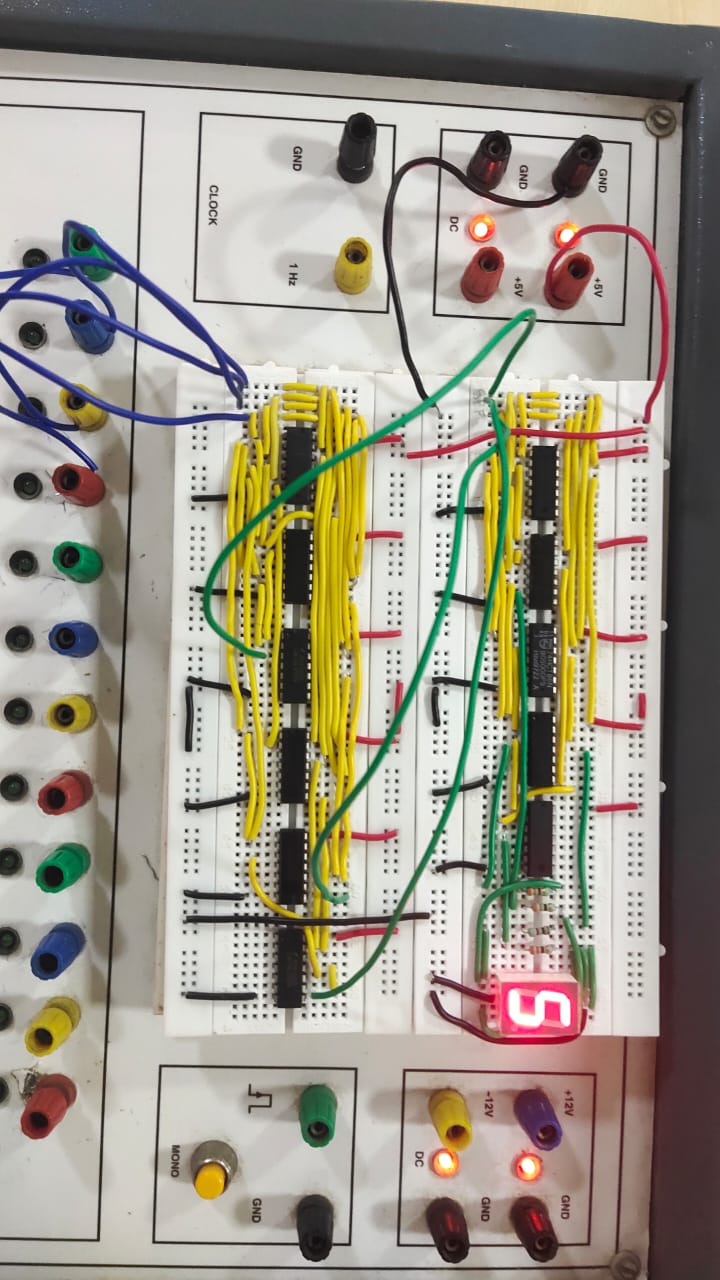


1. *Case 3 –*

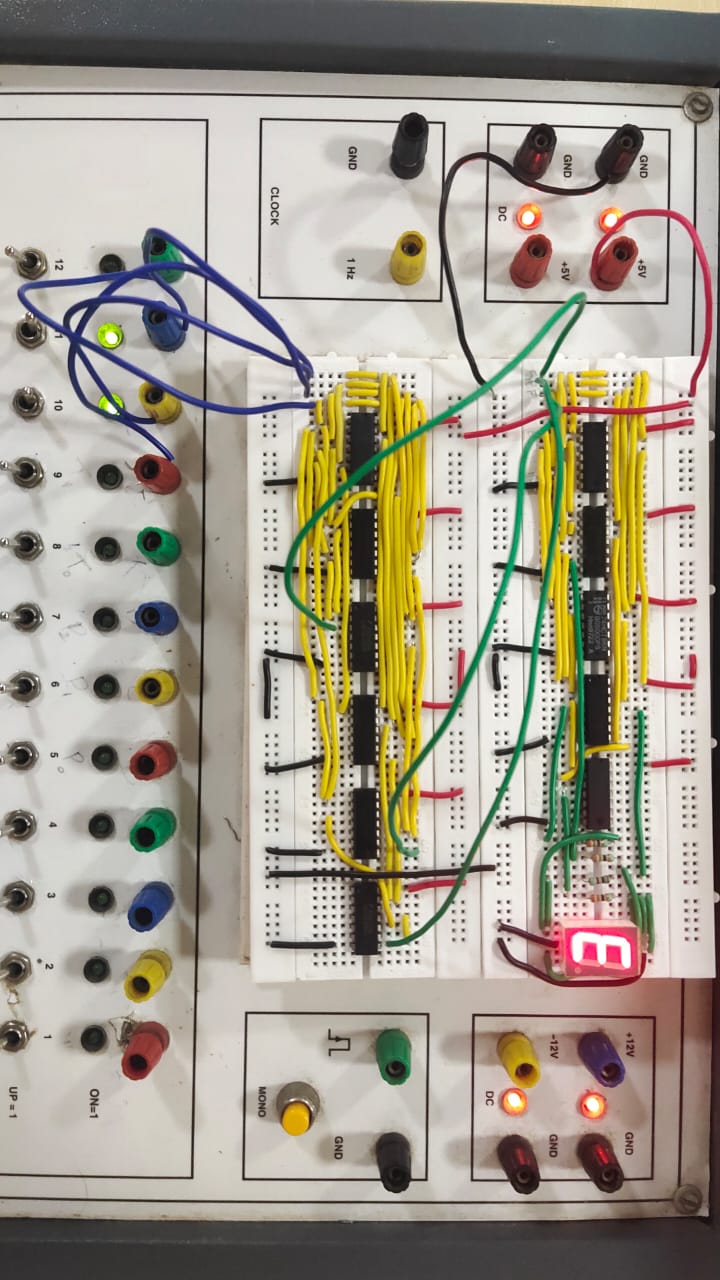


**Hardware Output:**

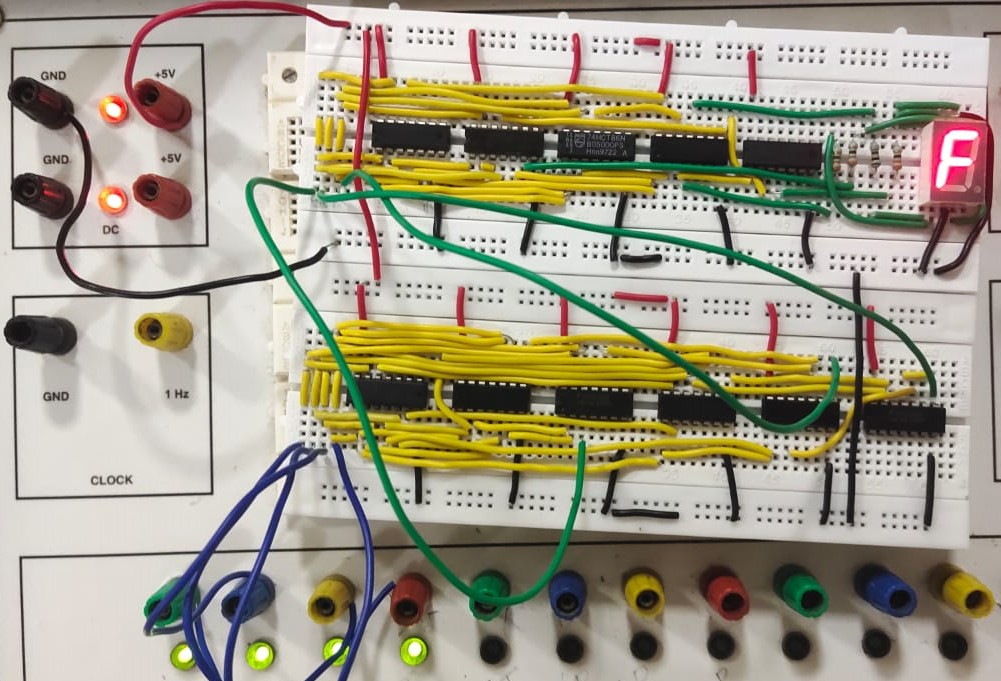
1. *Case 1 –*

**

1. *Case 2 –*



1. *Case 3 –*

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